Please amend the subject application as follows:

IN THE SPECIFICATION

Please amend the title of the invention as follows:

--MEMORY CELL INCLUDING STACKED GATE SIDEWALL PATTERNS AND METHOD FOR FABRICATING SAME--

Please amend the paragraph beginning at page 3, line 1 and ending at page 3, line 11 (¶ 0007) as follows:

--A memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance, a channel region defined between the source region and the drain region, a first charge storage layer formed on the channel region adjacent the source region, a second charge storage layer formed on the channel region adjacent the drain region, a gate ~~insulting~~ insulating layer formed on the channel region between the first and second charge storage layers, and a gate electrode formed on the gate insulating layer and the first and second charge storage layers.--

Please amend the paragraphs beginning at page 3, line 21 and ending at page 4, line 23 (¶¶ 0010-0011) as follows:

--Another memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a

predetermined distance, a channel region defined between the source region and the drain region, at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region, a gate ~~insulting~~ insulating layer formed on the channel region between the at least two charge storage layers, a gate pattern formed on the gate ~~insulting~~ insulating layer, at least one lower sidewall pattern formed on at least one of the at least two charge storage layers, and at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one upper sidewall pattern electrically contacts the at least one lower sidewall pattern and the gate pattern.

Another memory cell, in accordance with an embodiment of the present invention, comprises a source region and a drain region formed in a semiconductor substrate, wherein the source region and the drain region are separated by a predetermined distance, a channel region defined between the source region and the drain region, at least two charge storage layers formed apart from each other at a first position and a second position on the channel region, wherein the first position is adjacent the source region and the second position is adjacent the drain region, a gate ~~insulting~~ insulating layer formed on the channel region between the at least two charge storage layers, a gate pattern formed on the gate ~~insulting~~ insulating layer, at least one lower sidewall pattern formed on at least one of the at least two charge storage layers, and at least one upper sidewall pattern formed on the at least one lower sidewall pattern, wherein the at least one lower sidewall pattern is electrically insulated from the at least one upper sidewall pattern and the gate pattern.--

Please amend the paragraphs beginning at page 5, line 16 and ending at page 6, line 16 (¶¶ 0014-0015) as follows:

--Another method for fabricating a memory cell, in accordance with an embodiment of the present invention, comprises stacking an insulating layer, a lower conductive layer, an interlayer insulating layer and a mask layer on a semiconductor substrate, patterning the mask layer, the interlayer insulating layer, the lower conductive layer and the insulating layer to form a gap region, forming a gate oxide layer on exposed surfaces of the semiconductor substrate and the lower conductive layer in the gap region, forming a gate pattern on the gate oxide layer for filling the gap region, removing the mask layer to expose the interlayer insulating layer and sidewall portions of the gate pattern, forming an upper sidewall pattern on each exposed sidewall portion of the gate pattern and on the interlayer ~~insulting~~ insulating layer, patterning the interlayer insulating layer, the lower conductive layer and the insulating layer to form an inter-gate insulating layer, a lower sidewall pattern and a charge storage layer under each upper sidewall pattern, wherein the gate pattern and each upper sidewall pattern is used as an etching mask, and forming a source region and a drain region in the semiconductor substrate adjacent a first charge storage layer and a second charge storage layer, respectively, wherein the gate pattern and each upper sidewall pattern is used as an ion implantation mask.

Impurities may be doped into an exposed portion of the semiconductor substrate in the gap region to form a channel region. Forming the upper sidewall pattern on each exposed sidewall portion may comprise forming an upper conductive layer on the semiconductor substrate after removing the mask layer, and

anisotropically etching the upper conductive layer to expose the lower conductive layer or the interlayer ~~insulting~~ insulating layer.--

Please amend the paragraph beginning at page 8, line 6 and ending at page 8, line 18 (¶ 0025) as follows:

--As shown in FIG. 2, the charge storage insulating layer 72 is formed on the channel region 76 adjacent the source and drain regions 74s and 74d. The gate insulating layer 64 includes sidewalls 64s which are aligned with sidewalls of the charge storage insulating layer 72 and extend in the vertical direction. The gate electrode 70 includes a gate pattern 66 formed on the gate ~~insulting~~ insulating layer 64 and lower and upper sidewall patterns 58a and 68a, respectively. The lower and upper sidewall patterns 58a and 68a are stacked next to the sidewalls of the gate pattern 66 and on the charge storage insulating layer 72. A silicide layer 66s may be formed on top of the gate pattern 66. The gate insulating layer 64 extends to the region between the lower sidewall pattern 58a and the gate pattern 66. The gate pattern 66, the upper sidewall pattern 68a and the lower sidewall pattern 58a include a conductive layer and are electrically connected with one another.--

Please amend the paragraph beginning at page 10, line 23 and ending at page 11, line 16 (¶ 0034) as follows:

--Referring to FIG. 8, a SONOS memory cell includes source and drain regions 74s and 74d formed in a semiconductor substrate 50. Channel region 76 is located between the source and drain regions 74s and 74d. A gate insulating layer

64 and a charge storage insulating layer 72 are formed on the channel region 76, and a gate electrode 70 is formed on the gate insulating layer 64 and the charge storage insulating layer 72. The charge storage insulating layer 72 is formed on the channel region 76 adjacent the source and drain regions 74s and 74d. The gate insulating layer 64 includes sidewalls 64s which are aligned with sidewalls of charge storage insulating layer 72 and extend in the vertical direction. The gate electrode 70 includes a gate pattern 66 formed on the gate ~~insulting~~ insulating layer 64 and lower and upper sidewall patterns 58a and 68a, respectively, that are stacked next to the sidewalls of the gate pattern 66. The gate electrode 70 also includes an inter-gate insulating layer 59a interposed between the lower and upper sidewall patterns 58a and 68a. A silicide layer 66s may be formed on top of the gate pattern 66. The gate insulating layer 64 extends to the region between the lower sidewall pattern 58a and the gate pattern 66 and connects to the inter-gate insulating layer 59a. As a result, the lower sidewall pattern 58a is insulated from the gate pattern 66 and the upper sidewall pattern 68a.--

Please amend the paragraphs beginning at page 14, line 8 and ending at page 15, line 2 (¶¶ 0043-0044) as follows:

--A conventional SONOS memory cell may include a charge storage insulating layer formed on a channel region, wherein the charge storage insulating layer has an equivalent oxide thickness (EOT) that is larger than a thickness of gate insulating layer. In contrast, according to an embodiment of the present invention, a charge storage ~~insulting~~ insulating layer is formed only on the regions adjacent the

source and drain regions, and a thin gate ~~insulting~~ insulating layer is formed on the remaining portion of the channel region. With this configuration, the thin gate insulating layer has an EOT that is less than a thickness of the charge storage insulating layer.

In accordance with an embodiment of the present invention, the charge storage ~~insulting~~ insulating layer is formed only on the region where electrons are trapped, thereby improving an operating rate of the memory cell. In addition, a width of the charge storage insulating layer can be controlled to have a uniform thickness, such that distribution of the cell can be reduced. The charge storage ~~insulting~~ insulating layer may be formed in separate parts on different portions on the channel region (e.g., adjacent the drain and storage regions), thereby improving data identification between the charge storage regions. Furthermore, the width of the charge storage insulating layer along the channel length can be minute, such that electrons and holes can be injected into the same region.--